SIDO Buck Converter with Independent Outputs

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***Abstract*— The portable electronics market is rapidly migrating towards more compact devices requiring multiple high-integrity high-efficiency voltage supplies for empowering the systems. This paper demonstrates a single inductor used in a buck converter with two output voltages from an input battery with voltage of value 3V. The main target is low cross regulation between the two outputs to supply independent load current levels while maintaining desired output voltage values well within a ripple that is set by adaptive hysteresis levels. A reverse current detector to avoid negative current flowing through the inductor prevents efficiency degradation at light load.**

I. INTRODUCTION

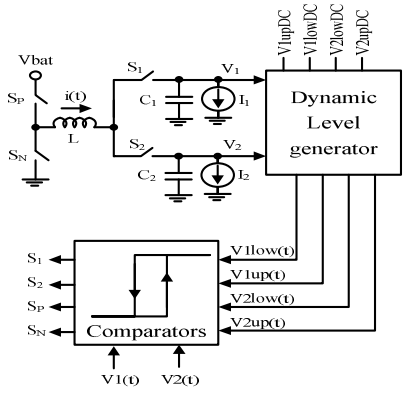
The typical buck converter is the most frequently used switched mode power supply (SMPS) in portable applications. Since multiple voltage rails are required on a Power Management IC (PMIC), several such converters are normally used in a device for obtaining different voltage levels. If a PMIC supplies N independent voltage rails, N such converters are required. The costliest and most area consuming component on the board of a SMPS design is the inductor. A solution for this issue is to use a single-inductor serving to multiple outputs [1-8]. A single-inductor dual output (SIDO) buck converter is shown in Fig. 1(a). Two independent outputs V_1 and V_2 are obtained from a single inductor L. C_1 and C_2 are output capacitors that maintain average load voltages V_1 and V_2 respectively, and provide output current when the inductor is serving the other output. The voltages $V_{1,2upDC}$, $V_{1,2lowDC}$, $V_{1,2up}(t)$ and $V_{1,2low}(t)$ are described in the following subsections. For the SIMO buck, T_1, T_2, … and T_N are the time windows for which L is connected to the outputs V_1, V_2, ... V_N, respectively. The timing diagram in Fig. 1(b) shows the different phases of operation of a SIDO buck converter. The slopes of inductor charge and discharge depend on the output that L is connected to for regulation. The time frames T_1 and T_2 are directly proportional to the load demanded at the respective output and are adjusted interactively by the feedback dynamic level comparator. For a buck converter switching at frequency f_s, output voltage V_o and ripple current Δi_L the value of the inductor is given as:

$$L = \frac{V_o(1-\frac{V_o}{V_{bat}})}{\Delta i_L f_s} \quad (1)$$

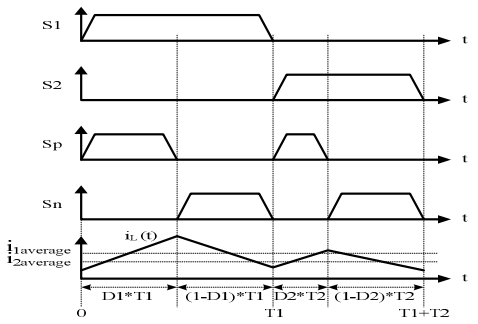
For the SIDO buck converter shown in Fig 1(a), since the inductor is shared between two outputs, L needs to be chosen so that the ripple current of the larger load output does not increase if the same switching frequency f_s is maintained:

$$L = \max\left(\frac{T_1 V_1(1-\frac{V_1}{V_{bat}})}{\Delta i_{L1}}, \frac{T_2 V_2(1-\frac{V_2}{V_{bat}})}{\Delta i_{L2}}\right) \quad (2)$$

In (2), Δi_{L1} and Δi_{L2} are the ripple currents, and are typically about 5-10% of the average rated loads I_1 and I_2 respectively. From (1) and (2) the advantage of sharing a single larger inductor in the SIDO converter is demonstrated. However, output capacitor value increases in the case of a SIDO buck converter in order to hold the voltage during the time window when the other output is being served by the inductor. This places a limitation on the total number of outputs that can be obtained using a single shared inductor. In this work, the excessive voltage discharge is alleviated by continuously monitoring the outputs and connecting the inductor to the output whose value has dropped low. Thus voltage ripple becomes more of a function of hysteresis monitoring levels than of the value of output capacitor.



(a)



(b)

Fig. 1 SIDO Buck Converter SMPS and Timing Diagram

II. CONTROL METHODOLOGY

In order to support low cross-regulation across independent load levels and achieve high output voltage accuracy, variable frequency control is chosen, for which dynamic hysteresis comparison levels are used. For each output, two dynamic levels $V_{1,2up}(t)$ and $V_{1,2low}(t)$ serve as thresholds against which the SIDO buck outputs are compared so that the voltage ripples are limited to within a set percentage of the reference voltages under all loading conditions. The hysteresis levels corresponding to the SIDO buck's outputs $V_{1,2}$ can be defined as follows:

$$V_{1,2up}(t) = V_{1,2upDC} - K_z \cdot \frac{dV_{1,2}(t)}{dt} \tag{3}$$

$$V_{1,2low}(t) = V_{1,2lowDC} - K_z \cdot \frac{dV_{1,2}(t)}{dt} \tag{4}$$

The derivative of the output voltages is a measure of inductor current; hence the threshold levels are dynamically adjusted according to I_L. The value of the coefficient K_Z determines the sensitivity of the dynamic levels. A very large value of K_Z causes high swing in the upper and lower dynamic levels and their possible overlap whereas a small value desensitizes the threshold levels to load current variations increasing the output voltage ripple.

Through minimized cross-regulation the proposed controller for the SIDO buck converter is able to supply the output at full load as well as the output at stand-by simultaneously while maintaining accurate output voltage values.

A. Ripple Control and Cross Regulation

The output voltages $V_{1,2}$ are limited to the hysteresis bands by comparing them with the dynamic levels to control the switches S_P and S_N. In Fig. 2, during T_1, when L is connected to one of the outputs, S_P is activated and its voltage variation is positive due to the current injected by the inductor. Based on the speed of the variation of the output voltage, the dynamic levels (3) and (4) are adjusted; large load current leads to large steps in the dynamic levels. Since I_L is positive, the threshold voltage $V_{1,2up}$ decreases thus preventing significant overshoot at the end of the S_P phase even in the presence of control circuit delays. In the following S_N phase one of the inductor terminals is grounded but continues to serve the output if L is sized sufficiently to support the total DC load. During T_2, the output voltage discharge at a rate given by $-I_{1,2}/C_{1,2}$. This causes a step increase in the dynamic levels, making it move closer to the output voltage profile. When switching from one output to the other, switch S_1 is closed if the voltage V_1 discharges to below $V_{1low}(t)$; i.e. S_1 and S_2 are controlled by load levels in the outputs. This guarantees that V_1 and V_2 stay well within the static bounds $V_{1,2upDC}$ and $V_{1,2lowDC}$. Thus the ripples of the output voltages are stronger functions of the static levels $V_{1,2upDC}$ and $V_{1,2lowDC}$ than of the external LC tank. This is an advantage from a form factor reduction point of view. Lower ripple requires closer static bounds, and also increases the frequency with which S_1, S_2, S_p, S_n switch.

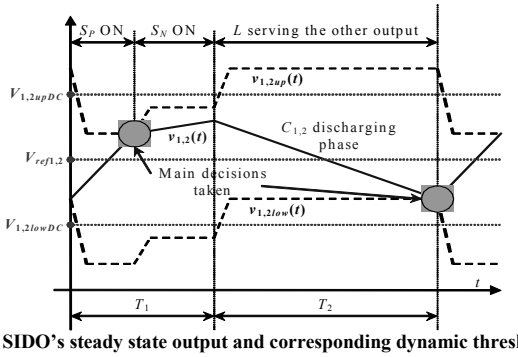


Fig. 2 SIDO's steady state output and corresponding dynamic thresholds

The time periods T_1 and T_2 are adjusted by the controller such that the average loads at both outputs are delivered over one time period when the converter is in steady state; i.e.

$$\frac{\int_0^{T_1} i_l(t)dt}{T_1 + T_2} = i_{1average} \quad \frac{\int_{T_1}^{T_2} i_l(t)dt}{T_1 + T_2} = i_{2average} \tag{5}$$

The issue of cross-regulation arises from the sharing of boundary conditions of inductor current between the output branches. This causes coupling between the sub-converters. If the inductor were to discharge to a state of zero current at the end of every time window, then independent load supply can be achieved at each output without undesirable rise or fall in voltage [1-4]. However, the disadvantage of operating the SIDO buck converter in this mode of discontinuous conduction for all load conditions is the rise in peak currents flowing through the inductor, increasing current stress of the switches and conduction losses as well as loss in system efficiency due to the full charge and discharge of additional parasitic capacitors. To decrease the peak inductor currents the inductor might be reset to a constant value I_{dc} instead of zero [5,6]. A variation of this technique is to reset the inductor to different current values that are dependent on the individual loads. This technique requires an additional low-resistance switch across the inductor. Further, current sensing circuits that are sensitive to high frequency noise are required. Control methodologies like Adaptive Delta Modulation [7] and Ordered Power Distributive Control [8] use digital algorithms and analog signal processing circuits to control the voltages. These solutions have a fixed frequency of operation which leads to the inability of the SIDO SMPS to regulate with widely varying load ranges at both outputs.

In order to meet the average load current requirements of both the outputs as set by (5), the time multiplexing of L is controlled. In Fig. 2, when $S_{1,2}$ is ON during T_1, $C_{2,1}$ discharges, causing $V_{2,1}$ to droop with a rate that is directly proportional to its load current. This causes an upward shift in $V_{2,1low}(t)$. At time

T_2 when V_1 hits $V_{2,1low}(t)$, $S_{2,1}$ is turned ON. Thus the output with higher load current takes priority since the transient voltage profile is monitored. L is connected for a longer time to the output with the higher load. The absence of any averaging circuits or any form of linear compensation leads to better transient performance.

B. Architecture and control flow

Fig. 3 shows the topology and control architecture of the SIDO buck converter. Eqns. (3) and (4) are implemented using analog differentiators with DC offsets. V_1 and V_2 are compared with the dynamic levels to generate the control signals for switches S_p and S_n. S_1 and S_2 are controlled by the comparator that sets the priority of the outputs based on the voltage error and load current, accordingly setting the flag 'M' to 1 or 0. The delays due to the control gates, drivers and comparators are negligible compared to the output time constant, leading to very small control loop delay. Reverse current is detected by monitoring voltages across S_1 and S_2 in order to avoid the flow of negative current flowing through the inductor. When the reverse current detector 'R' is high the switches S_n and S_{aux} are closed while all the other switches are immediately turned OFF. This switching action grounds the inductor terminals avoiding negative current flow through it and also prevents efficiency degradation, and the SIDO converter is in 'standby' and only the quiescent current by the control circuitry is consumed at this time. A high speed, high power reverse current comparator ensures faster inductor grounding action, minimizing the average loss of the system during discontinuous conduction. The flowchart shown in Fig. 4 summarizes the sequence of operations implemented by the digital controller. The two loops that control the battery side and load side switches work independent of each other, except in the event of reverse current flow. This independent operation guarantees the reliable operation of the control system. Standard digital logic is used to implement these operations.

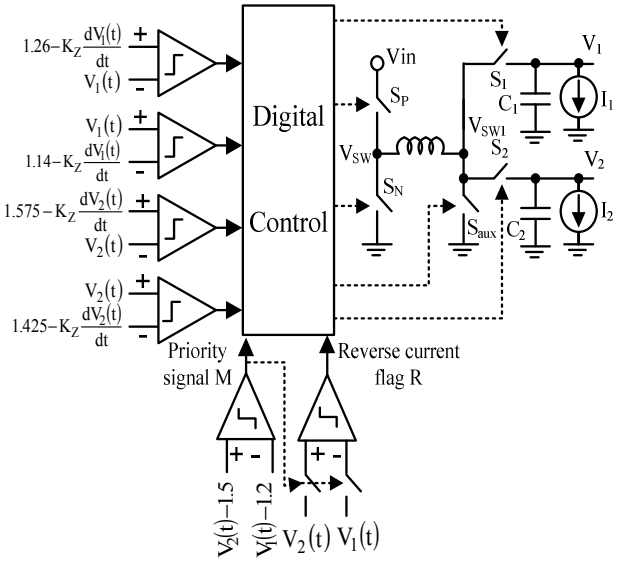


Fig. 3 SIDO system Overview

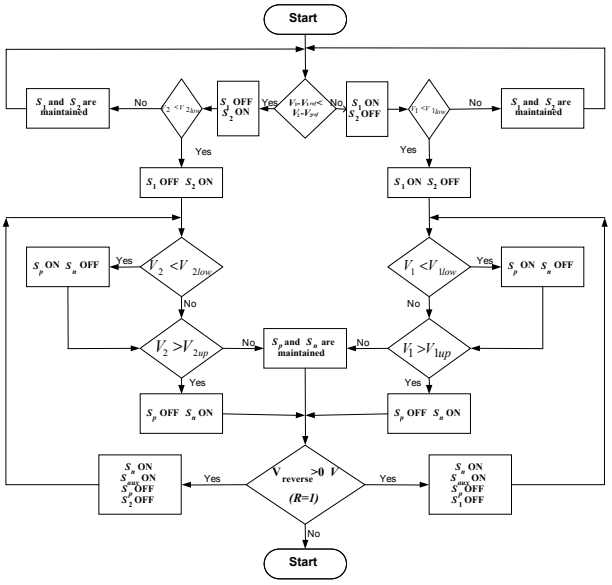


Fig. 4 Logical flow of operations in the SIDO Buck Converter

III. SCHEMATIC SIMULATION RESULTS

In this work, the value of L is1 µH and the values of the output capacitors are 4.7 µF each. The controller was designed and simulated at transistor level using a conventional 0.5 µm CMOS technology. When maximum load i.e. 300 mA is present at each output, the transient response of $V_1(t)$ and $V_2(t)$ with corresponding dynamic levels are shown in Fig. 5. Overshoots or undershoots about their designated static bounds are due to the response time of the loop control. The effective switching frequency of each sub-converter is 500 kHz

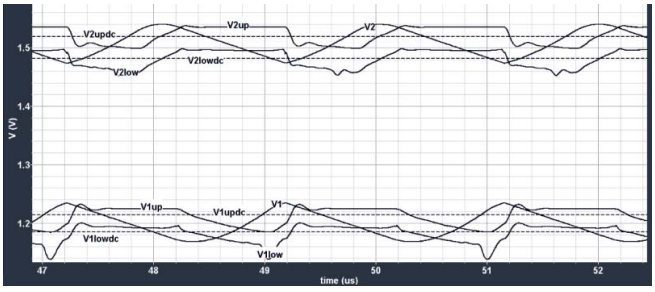


Fig. 5 Steady state V_1 and V_2 when load currents $I_1 = I_2 = 300$ mA

In Fig. 6, the load at $V_1(t)$ is 10 mA and at $V_2(t)$ is 300 mA. In Fig. 6, S_1 stays ON for just as long as the capacitor C_1 gets charged to over V_{1low}. Once the light load output V_1 is charged over its acceptable lower limit, the inductor is immediately connected to the output V_2 with the heavier load, and the switches S_p and S_n continue to get manipulated according to the corresponding dynamic thresholds. Hence both outputs with widely varied load values are served by the inductor thus minimizing the cross regulation. The sub-converter with heavy load switches at 500 kHz while the sub-converter with light load switches at 125 kHz.

Fig. 7 shows two families of curves; the dotted traces correspond to the output voltages with dynamic hysteresis, while

the solid lines indicate the outputs with static hysteresis. When dynamic levels are used the voltage ripple is better controlled within the permissible bounds. In the case of static hysteresis, a large output capacitor would be required to effectively control this ripple value.

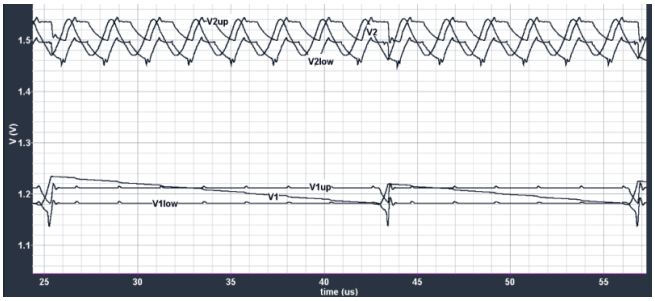


Fig. 6 Steady state V_1 and V_2 when load currents I_1 = 10mA and I_2 = 300 mA

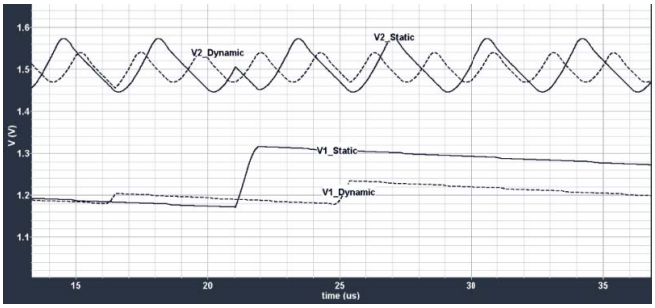


Fig. 7 Comparison of static and dynamic hysteresis

Fig. 8 shows the load regulation of $V_1(t)$ and cross regulation of $V_2(t)$. There is a step increase in the load current I_1 from 10mA to 300mA leading to an increase in the ripple frequency of $V_1(t)$ at the instant of the load step. This increase in the switching frequency ensures that the sudden load step is handled by the inductor energy, thus helping the loop recover without any undesirable dips in the output voltages.

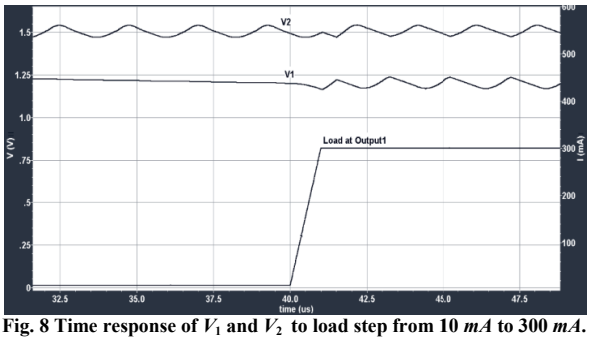


Fig. 8 Time response of V_1 and V_2 to load step from 10 *mA* to 300 *mA*.

Hence from simulations it can be concluded that frequency of operation is "adaptive" leading to faster switching during high loads and slower switching during low loads, leading to improved efficiency. Also, the problem of negative inductor current during discontinuous conduction mode is solved, with no ringing transients, due to the presence of the auxiliary switch. This switch along with the reduced frequency of switching at light loads prevent low efficiency while operating at lighter loads as is the case in conventional SMPS's . This leads to an almost flat efficiency-load curve as depicted in Fig. 9 that is desirable in many applications in order to optimize the performance of the power supply over a wide range of loads. Losses across all five switches in the SIDO converter are accounted for in the curve of Fig. 9 hence higher values of efficiency are achievable with more sophisticated technology.

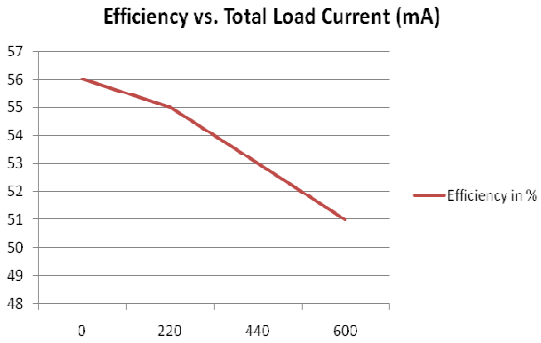


Fig. 9 Overall efficiency vs. total load current I_1 and I_2

IV. CONCLUSION

A single-inductor two-output switching regulator with low cross regulation, high accuracy and 2.5% ripple limits has been described. These achievements are a result of the proposed non linear hysteresis control applied to the SIDO buck converter leading to superior transient performance and disturbance rejection. Using the proposed dynamic hysteresis control methodology, constant efficiency values at different load combinations that is essential for optimum performance is achieved. The downside of the proposed method is the variation of the operating frequency with load. Nevertheless, the switching frequency can be controlled to stay within a band of acceptable frequencies by tuning the width of the hysteresis loop using an auxiliary feedback loop. The principles presented in this paper can be extended to a multiple output (n>2) buck converter.

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